Title: SYSTEM AND METHOD FOR DATA RETENTION WITH REDUCED LEAKAGE CURRENT

IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 2, line 15, is amended as follows:

Modern semiconductor processing technology has advanced rapidly with increased transistor density, reduced chip area and improved transistor performance. In many cases, these advancements have come at the expense of increased leakage power. In the past, this leakage power has been small in comparison to the total chip power; however, with advancing technologies, leakage power is becoming an increasingly larger percentage. Part of the reason for this increase in leakage power is that many newer technologies rely more on higher-leakage semiconductor devices, which may have shorter channel lengths, thinner gate-oxide layers and/or lower threshold voltages than semiconductor devices of more conventional processing technologies.

The paragraph beginning at page 8, line 4, is amended as follows:

In some embodiments, switching subcircuit 232, isolation subcircuit 222, and subcircuits 224 and 226 may operate during a standby mode and may comprise lower-leakage semiconductor devices. In these embodiments, pass-gate subcircuit 220 and inverter 230 may comprise higher-leakage semiconductor devices, and may be turned off in the standby mode. The higher-leakage semiconductor devices may provide better performance during non-standby operations. As can be appreciated, in a system[[,]] such as system 100 (FIG. 1) that may employ hundreds of thousands of circuits 200, the use of a standby mode may reduce current consumption considerably while retaining system state information.

Filing Date: June 27, 2003
Title: SYSTEM AND METHOD FOR DATA RETENTION WITH REDUCED LEAKAGE CURRENT

The paragraph beginning at page 11, line 15, is amended as follows:

In embodiments, the supply-switching subcircuit 432 may be a semiconductor device, such as a PMOS (P-channel metal-oxide semiconductor) device, which conducts when sleep signal 428 is low, coupling devices 424 and 426 to regular voltage supply 418. In these embodiments, switching subcircuit 432 and data-retention subcircuits 424 and 426 may have a well tap coupled with supplemental voltage supply 434. The well tap may allow current from the supplemental voltage supply to flow through the tap to data-retention subcircuits 424 and 426 when sleep signal 428 is high even though subcircuit 432 is not receiving regular voltage supply 418. In these embodiments, the current provided through the tap may be limited to the leakage current of data-retention subcircuits 424 and 426 when in standby mode, although the scope of the invention is not limited in this respect.